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NGUYEN, KIMBERLY D	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/015,965
Filing Date: November 30, 2001
Appellant(s): VINCENT, YANNICK

Vincent Yannick

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11 May 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-9 (Group I and II) do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

The copy of the appealed claims contained in the Appendix to the brief is correct.

6,574,776	Chiang	6/3/2003
5,978,822	Muwafi et al	11/2/1999

Van Rensburg et al (US 2003/0004891) "System for conducting commercial transactions", United States Patent Application Publication, 2 January 2003.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 5, 7, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Chiang (US 6,574,776).

Chiang teaches a data processing system, comprising:

a EDC/ECC-P processor 13/15, which serves as a microprocessor (see fig. 1),

a communication device communicating with an electronic module (i.e. memory unit 11, which serves as electronic module) intended to send a conventional signal to the microprocessor (i.e., providing data communication between memory unit 11 and the processors; see col. 1, line 66 through col. 2, line 26); and

a hardware circuit allowing an inversion an order of bits of a word as a function of a value of the conventional signal during a transfer of the word between the electronic module 11 and the microprocessor (fig. 7; col. 6, line 59 through col. 7, line 48).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang in view of Van Rensburg et al. (US 2003/0004891; hereinafter "Van Rensburg"). The teachings of Chiang have been discussed above.

Chiang fails to teach or fairly suggest the electronic module is a Subscriber Identity Module (hereinafter "SIM")card.

Van Rensburg teaches the electronic module 2 is a SIM card (fig. 2; paragraphs 41 and 50).

It would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to incorporate the SIM card as taught by Van Rensburg to the teachings of Chiang in order to employ memory card, such as SIM card, for conducting commercial transactions including a large number of participating system members.

5. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang in view of Muwafi et al. (US 5,978,822; hereinafter "Muwafi"). The teachings of Chiang have been discussed above.

Chiang fails to teach or fairly suggest the hardware circuit comprising a switch, a right shift register and a left shift register electrically connected to the switch.

Muwafi teaches a circuit which comprises switches (fig. 9, lines 19-25) and a post shift unit 80 to shift (to the left or right) the bits of each value processed (fig. 5; col. 8, lines 31-45).

It would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to incorporate the notoriously old and well known the order of bits of the word as taught by Muwafi to the teachings of Chiang in order to provide the instant system with a reduction of time for processing operations.

(11) Response to Argument

1. With respect to the Appellant's argument that "However, a proper understanding of Chiang reveals that memory unit 11 only sends data blocks to EDC processor unit 13 as evidenced by the illustration of data exclusively being sent from memory unit 11 to EDC processor unit 13." (see page 6, lines 2-4); the examiner respectfully requests the Appellant to further review the second limitation of the independent claims (1, 5 and 9) that claims "a communication device communicating with an **electronic module intended to send a convention signal to said microprocessor**"; wherein the electronic module is Chiang's memory unit 11, convention signal is Chiang's data blocks, and microprocessor is Chiang's EDC processor unit 13; which clearly meet the claimed language of the instant invention.

2. With respect to the Appellant's argument that "a proper understanding of Chiang reveals that (1) EDC Bit Order Inverter inverts EDC error detection bits d(k) from a left shift feedback register LSFR as opposed to the data block from memory unit 11, and (2) EDC Bit Order Inverter does **not** invert EDC error detection bus d(k) as a function of any signal as evidenced by

the failure of Chiang to illustrate a signal being inputted into EDC Bit Order Inverter for purposes of controlling the inversion of EDC error detection bits d(k)." (see page 6, lines 9-14); the examiner respectfully requests the Appellant to further review Chiang's reference that "An EDC error detection factor, which is appended to the data stream, is the ordered sequence of bit values remaining in the LFSR shown in fig. 6 after the entire data stream has passed through the LFSR." (col. 5, lines 22-25) and "The ordered sequence of 32 bit values remaining in the LFSR, after the data bit B[k] are all passed through the apparatus and through an EDC bit order inverter, is the 32-bit EDC factor, where 16 consecutive bits (a word) are processed consecutively for EDC purposes." (col. 6, lines 59-63); which serves as "a hard ware circuit allowing an inversion of an order of bits of word as a function of a value of the convention signal during a transfer of the word between the electronic module and the microprocessor" as set forth in independent claims of the claimed invention.

3. With respect to the Appellant's argument of claim in Group II that "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See, MPEP 2143. The Appellant respectfully traverses this obviousness rejection of claims 4 and 8, because Chiang teaches away from "wherein said hardware circuit includes: a switch; a right shift register electrically connected to said switch; and a left shift register electrically connected to said switch" as recited in dependent claims 4 and 8. Specifically, Chiang teaches away from an

incorporation of a switch within ED Bit Order Inverter **by failing to teach a conditional inversion of the EDC error detection bits d(k) by the ED Bit Order Inverter**." (see page 9, 2nd paragraph); the examiner respectfully disagrees with the Appellant because "The ordered sequence of 32 bit values remaining in the LFSR, after the data bit B[k] are all passed through the apparatus and through an EDC bit order inverter, is the 32-bit EDC factor, where 16 consecutive bits (a word) are processed consecutively for EDC purposes." (see fig. 7; col. 6, lines 59-63); which serves as the conditional inversion of the EDC error detection bits d(k) by the EDC Bit Order inverter.

4. In response to Appellant's argument that the references fail to show certain features of Appellant's invention, it is noted that the features upon which Appellant's relies (i.e., If the value of the convention signal is "0", then hardware circuit does not invert the order of the bits of a word during a transfer of the word from electronic module to microprocessor via communication device in the form of [BYTE1] and [BYTE2] whereby the order of the bits of the word in the form of [BYTE1] is identical to the order of the bits of the word in the form of [BYTE2]. Similarly, if the value of the convention signal is "0", then hardware circuit does not invert the order of the bits of a word during the transfer a word from microprocessor to electronic module via communication device in the form of [BYTE3] and [BYTE4] whereby the order of the bits of the word in the form of [BYTE3] is identical to the order of the bits of the word in the form of [BYTE4]..." (see page 3, lines 6-19)) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

KDN
August 3, 2004

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